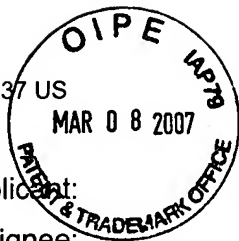


X-1337 US



PATENT

IN THE UNITED STATES PATENT OFFICE

Applicant: Gareth D. Edwards

Assignee: Xilinx, Inc.

Title: "Scheme for Eliminating the Effects of Duty Cycle Asymmetry in Clock-Forwarded Double Data Rate Interface Applications"

Serial No.: 10/703,813 File Date: 11-12-2003

Examiner: Fritz Alphonse Art Unit: 2133

Docket No.: X-1337 US Conf. No.: 6961

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

FILED WITH RCE

Dear Sir:

Pursuant to 37 C.F.R. 1.56, Applicant brings to the attention of the Examiner the one (1) reference listed in the attached Substitute for Form 1449A/PTO. A copy is enclosed herein.

This Information Disclosure Statement is being filed with an RCE under 37 CFR 1.114 along with the fee requirements set forth under 37 CFR 1.17(e).

Citation of the above document shall not be construed as an admission that the document is necessarily prior art with respect to the instant invention. Citation of the above document shall not be construed as a representation that a search has been made other than as described above. Also, the citation of the above document shall not be construed as an admission that the information cited herein is, or is considered to be, material to patentability as defined in §1.56(b).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on March 6, 2007.

Julie Matthews
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